SEMICONDUCTOR APPARATUS HAVING A CHARGE PUMP CIRCUIT

FIELD OF THE INVENTION

The invention relates to a semiconductor apparatus having a charge pump circuit, and more particularly to a semiconductor apparatus having a charge pump circuit which includes MOS type charge pump capacitors.

BACKGROUND OF THE INVENTION

Semiconductor apparatuses such as an LCD driver which has a low-voltage logic and a high-voltage logic on the same semiconductor chip are designed to generate a high voltage by stepping up a low-voltage of a low voltage supply using a charge pump circuit.

Fig. 1 illustrates such a charge pump circuit 11, in which a high voltage Vo (15 V) is obtained for a load 12 by stepping up a low voltage supply Vcc (about 3 V) of the power supply 13. As shown in Fig. 1, the charge pump circuit 11 has: p-type MOSFETs Q1 - Qn connected in series between an input terminal IN and an output terminal OUT; series inversion buffer circuits B1 - Bn for supplying gate voltages to the respective MOSFETs Q1 - Qn; capacitors C1 - Cn each having one end connected with a respective MOSFET (Q1 - Qn) or with the output terminal OUT; series inversion buffer circuits B1a - Bn-1a for supplying, predetermined voltages to the respective capacitors Q1 - Qn; inversion buffer circuits B1 - Bn; and an oscillator circuit OSC for providing clock signals to the inversion buffer circuits B1a - Bn-1a, the clock signals switching between predetermined high and low levels. (Capacitors C3 through Cn-1 and inversion buffer circuits B3 through Bn-1a are not shown.) The capacitor Cn in the last stage may be external to the charge pump circuit as shown in Fig. 1, if necessary, when large power is required by the load.

In operation, the charge pump circuit 11 generates a low (L) output at the output of the inversion buffer circuit B1 to thereby turn on the MOSFET Q1 when the output of the oscillator circuit OSC is high (H), and causing the output of the inversion buffer circuit B2 to become H to thereby turn off the MOSFET Q2. The outputs of the inversion buffer circuit B1a and the B2a are L and H, respectively. Consequently, the capacitor C1 is charged to the supply voltage Vcc.

Next, as the output of the oscillator circuit OSC goes low L, the output of the inversion buffer circuit B1 goes high H, thereby turning off the MOSFET Q1, while the output of the inversion buffer circuit B2 goes low L, thereby turning on the MOSFET Q2. At this stage, the output levels of the inversion buffer circuits B1a and B2a are H and L, respectively. Consequently, as a result of charge conservation principle, the capacitor C2 is charged with the charged voltage (Vcc) of the capacitor C1 plus the high output (Vcc) of the inversion buffer circuit B1a, thereby creating two times the supply voltage Vcc across the capacitor C2.

In this way, at every inversion of the oscillator circuit OSC between H and L levels, capacitor Cn acquires a voltage stepping up towards the required voltage Vo for the load 12.

Thus, in forming a charge pump circuit on one semiconductor chip together with a low-voltage circuit (not shown), their capacitors C1 - Cn-1 are mostly MOS capacitors, aligned in shape and size with other MOS transistors.

Such MOS capacitors are described in detail below with reference to Figs. 2 and 3. An N-well region 21 is formed on a p-type semiconductor substrate (referred to as substrate) 20. Formed within the N-well region 21 are N$^+$ regions 22-1 and 22-2 which are enriched with impurity to provide a higher conductivity. Formed on an insulating oxide layer (not shown) which

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overlies the N-well region 21, and between the N^+ regions 22-1 and 22-2, is a gate electrode 23. If a p-type MOSFET were formed on the N-well region 21, the N^+ regions 22-1 and 22-2 would make a p^+-type drain and a source, respectively, and the N-well region 21 between the N^+ regions 22-1 and 22-2, a channel region. (The N-well region will be hereinafter sometimes referred to channel region.)

A gate electrode 23 is connected with a lead wire 24 (which is an aluminum wiring layer 26 in Fig. 3) for connection with the terminal T1. The N^+ regions 22-1 and 22-2 are connected with a common lead wire 25 (which is an aluminum wiring layer 27 in Fig. 3) to maintain the regions at the same potential and to connect the regions with the terminal T2. Thus, a capacitor is provided between the gate electrode 23 and the N^+ regions 22-1 and 22-2, serving as a MOS capacitor. Similar capacitors are formed between the two wiring layers 26 and 27 and between the wiring layer 27 and the gate electrode 23, however, their capacitances are not important. In addition, oxide layers 28-1 and 28-2 are provided on the opposite ends of the N-well for isolation thereof from adjacent N-wells.

The magnitudes of these capacitances are not very large that they may not be sufficient for building up the required charging voltage when the power consumed by the load 12 is large. In that case, in order to provide sufficiently large power at all times, the switching frequency of the MOSFETs Q1 - Qn, i.e. the frequency of the oscillator circuit OSC, must be set high.

Unfortunately, the MOS capacitors as shown in Figs. 2 and 3 have a disadvantageous characteristic (hereinafter referred to as voltage dependent characteristic) that their capacitances vary with the voltages applied thereto. This is because the capacitance of the MOS capacitor is determined by the sum of two series capacitances, that is, the capacitance of the dielectric gate

oxide layer and the capacitance of the channel region (e.g. capacitance of the depletion layer) which depends on the physical condition of the channel region.

Although the capacitance of the gate oxide layer depends on the thickness thereof, it has a fixed value in that it has no voltage dependence. The capacitance of the channel region, on the other hand, depends on the physical conditions of the channel region, which in turn depends on the voltage applied thereto in different ways. For example, it depends on whether the channel is formed or not, and the thickness of the channel formed. Thus, the MOS capacitance depends on the voltage.

Of course the voltage dependence of the MOS capacitor would not matter so long as the capacitor can build up a sufficiently large voltage. However, a MOS capacitor for a charge pump circuit is subjected to frequent charging and discharging, and hence its voltage is always changing. Particularly, the voltage impressed on the first stage MOS capacitor is low and the resistance of the N-well region 21 forming the channel is large, so that it requires a fairly long time to gain an appreciable capacitance subsequent to the application of the voltage, thereby exhibiting a poor frequency response.

Fig. 4. shows such voltage dependent characteristic of the MOS capacitor for a switching frequency SW.f of 1 MHz. In Fig. 4, the abscissa represents the voltage Vg across the terminals T1 and T2 of a MOS capacitor. The ordinate represents the capacitance C of the MOS capacitor. The voltage Vg is applied across the terminals T1 and T2, with the terminal T1 being positive.

The static saturation capacitance of the MOS capacitor is about 750 pF as shown by a dotted line in Fig. 4. It is seen that the voltage dependence is saturated in the range from 2 V to 3 V. However, the rise of the capacitance

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is not steep and its saturated level is lower than the static capacitance due to high switching frequency. This characteristic varies with switching frequency.

The frequency response of the MOS capacitor may be improved through an additional manufacturing step of minimizing the resistance of the electrodes and modifying the characteristics of the N-well.

It is, however, not quite easy to change only the resistance of the electrodes and the characteristic of the N-well because the MOS capacitors are formed in the process of manufacturing the MOSFETs. Besides, if the change were possible, it would require time and cost.

Hence, the MOS capacitors has drawbacks that their voltage dependence limits the stepping up performance of the charge pump circuit.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a semiconductor apparatus including a charge pump circuit charged by MOS capacitors having improved frequency response. Thus, the invention can overcome the voltage dependence of the MOS capacitors if operated at a high frequency, thereby ensuring step-up performance of the charge pump circuit.

In accordance with one aspect of the invention, there is provided a semiconductor apparatus having a charge pump circuit which includes MOSFETs and MOS capacitors formed on the same substrate, wherein at least one of the MOS capacitors comprises:

a multiplicity of first electrodes formed at multiple locations within one region of the substrate;

insulating layers formed on/above respective substrate regions between neighboring first electrodes, each layer covering at least the

respective substrate region; and

a multiplicity of second electrodes formed on/above the respective insulating layers.

It is noted that the first electrodes are formed at multiple sections in a region of the substrate on the same side as the MOS capacitor to lower the resistance of the MOS capacitor, so that the frequency response itself is improved even if the voltage dependence continues to exist. Accordingly, the step-up performance of the charge pump is secured through the improvement of the frequency responses of the MOS capacitors even under a high frequency voltage.

The above mentioned one region has a specified conduction type and is isolated from other regions by isolation regions. The first electrodes can be formed on the semiconductor by locally increasing the conductivity of the regions reserved for the first electrodes. The insulating layer can be an insulating oxide layer.

The first electrodes may be elongate parallelly running rectangles. The second electrodes, each associated with a corresponding first electrode, may be formed elongate rectangles extending between two first electrodes. Each of the first electrodes may be provided with a highly conductive section that can be electrically coupled together.

The first electrodes may be provided with a first common wiring layer for electrically coupling the first electrodes together at one ends thereof, and with a second common wiring layer for coupling the second electrodes together at the other ends of the second electrodes. The first electrodes may be provided with a multiplicity of such first wiring layers for additional coupling.

Similarly, the second electrodes may be provided with a multiplicity of such second wiring layers for additional coupling.

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By forming the MOS capacitors in the arrangement as mentioned above, they can be fabricated simultaneously with other elements including MOSFETs.

A MOS capacitor of the invention can be used effectively in a charge pump circuit, especially in the first stage where the voltage dependent characteristic is significant under a given voltage. With the improvement of the voltage dependent characteristic by the MOS capacitor, the step-up performance of the charge pump circuit is greatly improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagramatic representation of a typical charge pump circuit.

Fig. 2 is a top view of a conventional MOS capacitor used in a charge pump circuit.

Fig. 3 is a cross sectional view of the MOS capacitor of Fig. 2.

Fig. 4 is a graphical representation of the voltage-capacitance characteristic of a conventional MOS capacitor of a charge pump circuit.

Fig. 5 is a top view of a MOS capacitor for use in a charge pump circuit according to the invention.

Fig. 6 is a cross sectional view of the MOS capacitor of Fig. 5.

Fig. 7 shows an equivalent circuit of a MOS capacitor useful in explaining the operation of the inventive MOS capacitor shown in Fig. 5.

Fig. 8 is a graphical representation of the voltage-capacitance characteristic of the MOS capacitor of Fig. 5.

Fig. 9 is a top view of a further MOS capacitor for use in a charge pump circuit according to the invention.

Fig. 10 is a top view of a still further MOS capacitor for use in a charge pump circuit according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention will now be described in detail by way of example with reference to the accompanying drawings.

Referring to Figs. 5 and 6, there is shown a MOS capacitor of one embodiment of the invention, used in a charge pump circuit formed together with other elements such as MOSFETs on the same semiconductor substrate of a semiconductor apparatus. Particularly, Figs. 5 and 6 schematically show the top view and the cross sectional view, respectively, of the MOS capacitor of the invention.

Fig. 7 shows an equivalent circuit of a MOS capacitor, representing the operation of the MOS capacitor. Fig. 8 compares voltage-capacitance characteristic of an inventive MOS capacitor with that of a conventional MOS capacitor.

As shown in Figs. 5 and 6, an N-well region 51 is formed on a p-type substrate 50. The N-well region 51 is surrounded by isolation regions in the form of, for example, oxide layers 58-1 and 58-2 to electrically isolate the MOS capacitor from other elements on the substrate. Such isolation regions can be provided not only by the oxide layers, but also by different means such as isolation trenches.

In addition to N^+ regions 52-1 and 52-6 serving as electrodes in a manner similar to conventional ones, there are provided, on the surface of the N-well region 51, four elongate N^+ regions 52-2 through 52-5 serving as electrodes. Thus, five (n=5) inter-electrode regions are defined on the N-well regions 51 between the six N^+ regions, i.e. six electrode regions 52-1 through 52-6. These N^+ regions 52-1 - 52-6 are connected at one ends thereof with an equipotential lead wire 55 (which is shown as an aluminum wiring layer 57 in

Fig. 6) extending to the terminal T2.

On the other hand, five gate electrodes 53-1 - 53-5 are formed on insulating oxide layers (not shown) which overlie the respective N-well regions, and which in turn locate between N^+ regions 52-1 - 52-6. Preferably, these gate electrodes 53-1 - 53-5 partly overlap the respective N^+ regions 52-1 - 52-6 via the insulating oxide layer (not shown). The electrodes 53-1 - 53-5 are connected at one ends thereof with an equipotential lead wire 54 (which is shown in Fig. 6 as an aluminum wiring layer 56) extending form the terminal T1. Crosses in Fig. 5 represent contact points of the lead wires.

Thus, in this arrangement, capacitors are formed between the gate electrodes 53-1 and a pair of N^+ regions 52-1 and 52-2;
between the gate electrode 53-2 and a pair of N^+ regions 52-2 and 52-3;
between the gate electrode 53-3 and a pair of N^+ regions 52-3 and 52-4;
between the gate electrode 53-4 and a pair of N^+ regions 52-4 and 52-5, and
between the gate electrode 53-5 and a pair of N^+ regions 52-5 - 53-6.

These capacitors are connected in parallel to serve as MOS capacitors between the two terminals T1 and T2. Although similar capacitors are formed between the two wiring layers 56 and 57, between the wiring layer 57 and the gate electrodes 53-1 - 53-5, their capacitances are not very large.

The operation of inventive MOS capacitors of a charge pump circuit will now be described in comparison to conventional ones.

In the MOS capacitors shown in Figs. 5 and 6, the resistance of an N-well 51 of the channel region is far greater than those of the gate electrodes 53-1 - 53-5. As an example, the sheet resistance of the gate electrodes 53-1 - 53-5 is 10 $\Omega/\square$, and the resistance of the N-well 51 is 1 k$\Omega/\square$.

Based on this example, resistances of a conventional MOS capacitor and that of the invention can be calculated as follows. First, assuming that a

MOS capacitor has a width L and a length H, one obtains for conventional MOS capaeitor;

Gate resistance Rg: $(H/L) \times 10\Omega$

N-well resistance Rn/w: $(L/H) \times (1/2) \times 1k\Omega$

For brevity, further assume that H = L.   Then, the above formula result in;

Gate resistance: $Rg = 10\Omega$, and

N-well resistance: $Rn/w = 500\Omega$

The equivalent circuit of this conventional MOS capacitor is shown in Fig. 7A. The symbol C represents the capacitance of the MOS capacitor.   The symbol w represents the number of electrodes, which is 2 in the example shown.

On the other hand, in the invention, capacitance is divided into five MOS capacitors in five branches (referred to as divided capacitors).   Based on the same assumption that the width and the length are L and H, respectively, one obtains;

Gate resistance Rg1 : $\{H/(L/5)\} \times 10\Omega$

N-well resistance Rn/w1: $\{(L/5)/H\} \times (1/2) \times 1k\Omega$

Assuming that H = L for brevity, one obtains;

Gate resistance: $Rg1 = 50\Omega$, and

N-well resistance: $Rn/w1 = 100\Omega$

An equivalent circuit of the inventive step-up circuit is shown in Fig. 7B. The symbol C1 represents the divisional MOS capacitance.   In this arrangement, the MOS capacitance is distributed over five parallel divisional MOS capacitors of capacitance C1 connected in series with a gate resistance Rg1 and an N-well resistance Rn/W1.   It is noted that MOS capacitors as a whole have the same frequency response as each MOS capacitor, so that the frequency characteristic of one MOS capacitor need be examined.   It would be clear that the total capacitance for the charge pump circuit having n stages is

given by the sum of these divisional MOS capacitors.

Thus, in the example shown herein, N-well resistance Rn/w1 is reduced (from 500Ω to 100Ω), and so is the sum of the gate resistance Rg1 and N-well resistance Rn/w1 (from 510Ω to 150Ω).

Next, referring to Fig. 7A, the frequency characteristic of a voltage dependent conventional MOS capacitor of capacitance C in series with a gate resistance Rg and an N-well resistance Rn/w will now be described.

First, it is noted that charging of the MOS capacitor charged by a voltage applied across the terminals T1 and T2 is slowed down by the voltage drop due to the gate resistance Rg and the N-well resistance Rn/w. Degree of the slowing depends on the magnitudes of the gate resistance Rg and the N-well resistance Rn/w. Second, because of the slowing down of charging, the capacitance C of the MOS capacitor must remain voltage dependent for a long period.

In comparison of the inventive MOS capacitor as shown in Figs. 5 and 6 to the prior art MOS capacitor as shown in Figs. 2 and 3, it is seen that the sum of the gate resistance Rg1 and the N-well resistance Rn/w1 of each branch is reduced (from 510Ω to 150Ω) than that of the conventional one, and so is the capacitance C1 of each branch. As a result, the inventive MOS capacitors have a shorter time constant of charging and hence they are charged quickly. This means that the time in which capacitance C1 of a MOS capacitor remains voltage dependent becomes shorter. If it is assumed that all the divisional MOS capacitors have the same gate resistance Rg1, N-well resistance Rn/w1, and MOS capacitance C1, the electric potentials at the points indicated by each broken line are the same, as seen in Fig. 7B. Hence, these equipotential points may be connected. Of course they can be left disconnected.

Thus, the invention provides five divisional MOS capacitors C1 by forming five N-wells 51 between the respective six N$^+$ regions 52-1 - 52-6 serving as the electrodes of one polarity and five gate electrodes 53-1 - 53-5 of another polarity, such that the parallel divisional MOS capacitors C1 as a whole serve as a large MOS capacitor for the charge pump circuit.

In this way, the sum of the gate resistance Rg and the N-well resistance Rn/w is reduced to decrease undesirable frequency response that would be otherwise caused by the resistances Rg and Rn/w. Accordingly, although the capacitance of each MOS capacitor is voltage dependent, the frequency response of the MOS capacitor is improved. This is the case even for high frequency operation of the charge pump circuit, so that the step-up performance of the charge pump circuit is secured.

Fig. 8 illustrates the voltage-capacitor characteristic (solid curve) of an inventive MOS capacitor in comparison with a prior art MOS capacitor (broken curve). As in Fig. 4, Fig. 8 shows the characteristic of the exemplary MOS capacitors for a switching frequency of 1 MHz. The abscissa represents applied voltage Vg across the terminals T1 and T2 with the terminal T1 being positive. The ordinate represents capacitance C.

Although the inventive MOS capacitor has a little voltage dependence, it attains a large capacitance close to the static (saturation) capacitance of about 750 pF (dotted line) under a relatively low applied voltage (about 2 V) even when the switching frequency is as high as 1 MHz. That is, the MOS capacitor has a saturation capacitance close to that of the static capacitance (i.e. capacitance for zero frequency).

In the example shown herein, the number n of regions between the N$^+$ regions is 5. It would be apparent, however, that the number is arbitrary, and n can be any number greater than 1.

In the example shown herein, the N^+ regions 52-1 - 52-6 have elongate rectangular shapes and extend in parallel with one another. However, they are not limited to this arrangement. For example, they may have an extra N^+ region 52A at one ends thereof for connection with the neighboring regions as shown in Fig. 9.

In stead of connecting the gate electrodes 53-1 - 53-5 together at the other ends thereof by the lead wire 54, they can be connected together by further lead wires 54 which extend from the lead wire 54 over the respective gate regions and are connected to the respective regions at multiple points, as shown in Fig. 9.

It is possible to provide a multiplicity of recessed areas formed on the N^+ gate regions 53-1 - 53-5 between the N^+ regions 52-1 - 52-6 and a multiplicity of dotted N^+ regions 52B formed on the respective recessed areas to serve as electrodes as shown in Fig. 10. The dotted N^+ regions 52B can be then connected by longitudinally extending lead wires 55.

Provision of the N^+ regions 52A at one ends of the respective N^+ regions 52-1 - 52-6 for connecting them together, longitudinally extending lead wires 54 for connected with the gate electrodes 53-1 - 53-5, and the multiplicity of dotted N^+ electrode regions 52B between the N^+ regions 52-1 - 52-6, as shown in Figs. 9 and 10, will further improve the frequency response of the MOS capacitors.

Incidentally, provision of such extra N^+ regions results in a decrease in effective area of the gate electrode so that the area of the MOS capacitor must be increased by that amount used up for the extra N+ regions in order to secure the same capacity as a conventional one. To do this, capacitors in the later half stages of the charge pump circuit, especially one in the last stage, may have a different structure than that of an inventive MOS capacitor.

Effective application of the inventive MOS capacitor to a charge pump circuit is to use the MOS capacitor in the early stages of the circuit as shown in Fig. 1 where the capacitance C still has a voltage dependence under a given applied voltage, i.e. the Vg-C characteristic is not saturated yet. Therefore, it is preferred to use the inventive MOS capacitor in the first stage of the charge pump circuit where the capacitor is subjected to a low voltage.